

DAQ/Electronics Update

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DAQ/Electronics Personnel

- APD Module (UMN, IU) Roger Rusack, Tom Chase, Stuart Mufson, Jon Urheim, Walt Fox, Gerard Visser, Leon Mualem
- FEB (Harvard) John Oliver, Nathan Felt, Sarah Harder
- Power Distribution (UVa) Craig Dukes, Ken Nelson, Andrew Norman, Harvey Sugarman
- Power Removal (UMN) Bill Gilbert
- DAQ Hardware (FNAL) Vince Pavlicek, Rick Kwarcianny, Bill Haynes
- DAQ Software (FNAL) Jerry Guglielmo, Kurt Biery
- DAQ integration (FNAL) Margaret Votava
- Detector Control System (UVa) Andrew Norman

- My apologies to anyone I missed

APD Module

- APD--See Roger's Talk up next
- Testing of Indiana Thermal/Mechanical prototypes continues
 - Critical for determining system heat load
 - Developing design for production module
 - See Jon Urheim's talk Friday (and yesterday)
 - More design required, but moving forward

Front-End Board

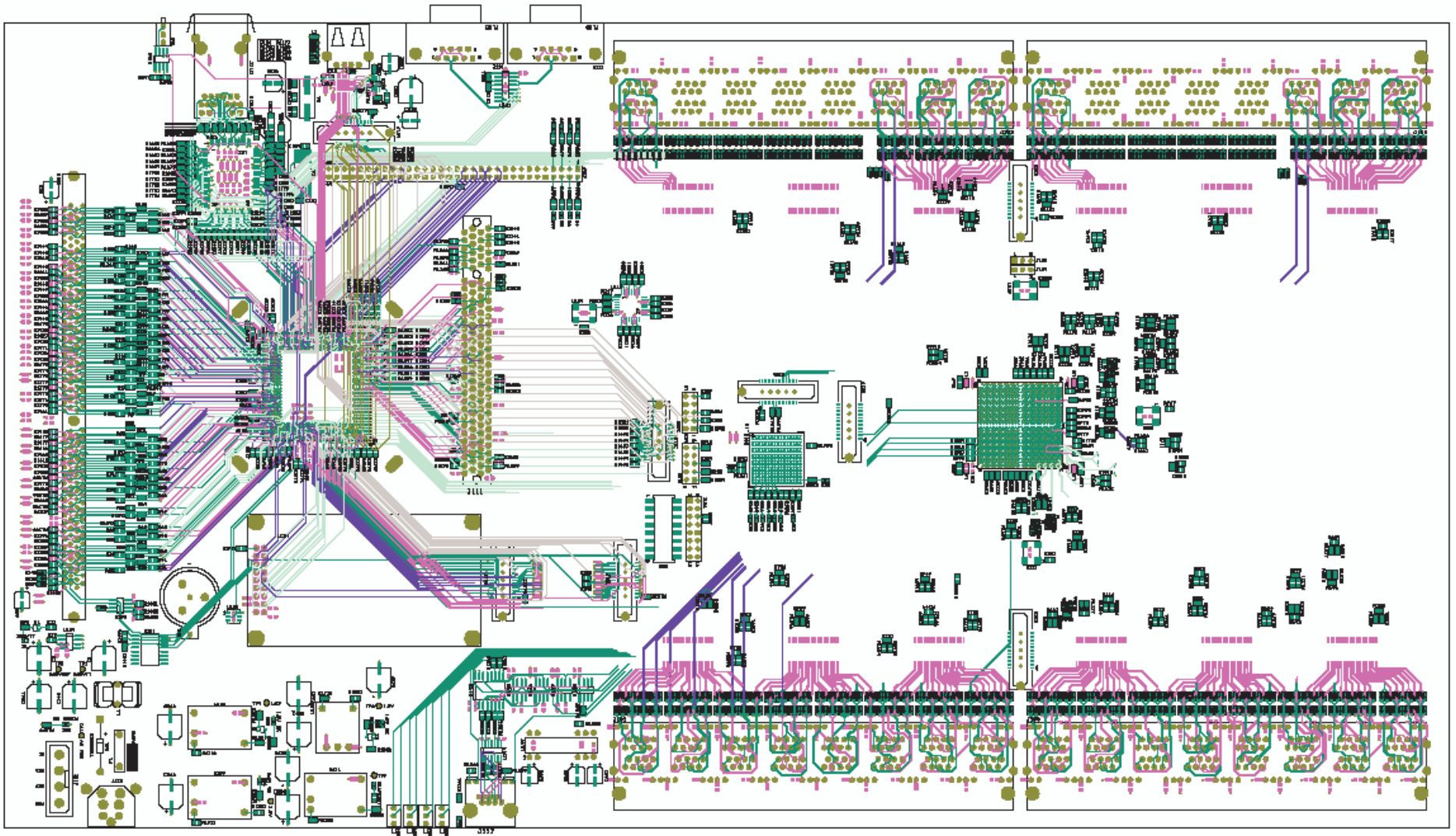
- Standalone ASIC tests completed by Tom Zimmerman
 - Excellent performance bare chip tested at 110electrons RMS, simulated to be 150.
 - Packaging decided
 - Will be tested on the next prototype readout board
- Schematic design for version P2.0 of the FEB was developed in July.
 - This version will contain the following features.
 - ChipIdeas quad ADC which was tested under P1.0
 - TEC control circuit as supplied by Gerard Visser
 - On board FPGA controller with Cypress USB interface chip
 - Interface cable to APD module
- These boards are intended to service and read out multiple APD modules and NOvA detectors.

Data Concentrator Module

Prototype Development Status

- Schematic is complete and has passed an internal review.
- PC board layout is well under way. Parts are placed and routing is about 70% complete.
- Parts for five boards have been ordered. About a third of the parts have arrived.
- Software and firmware development not yet started.

Data Combiner Module (In Progress)



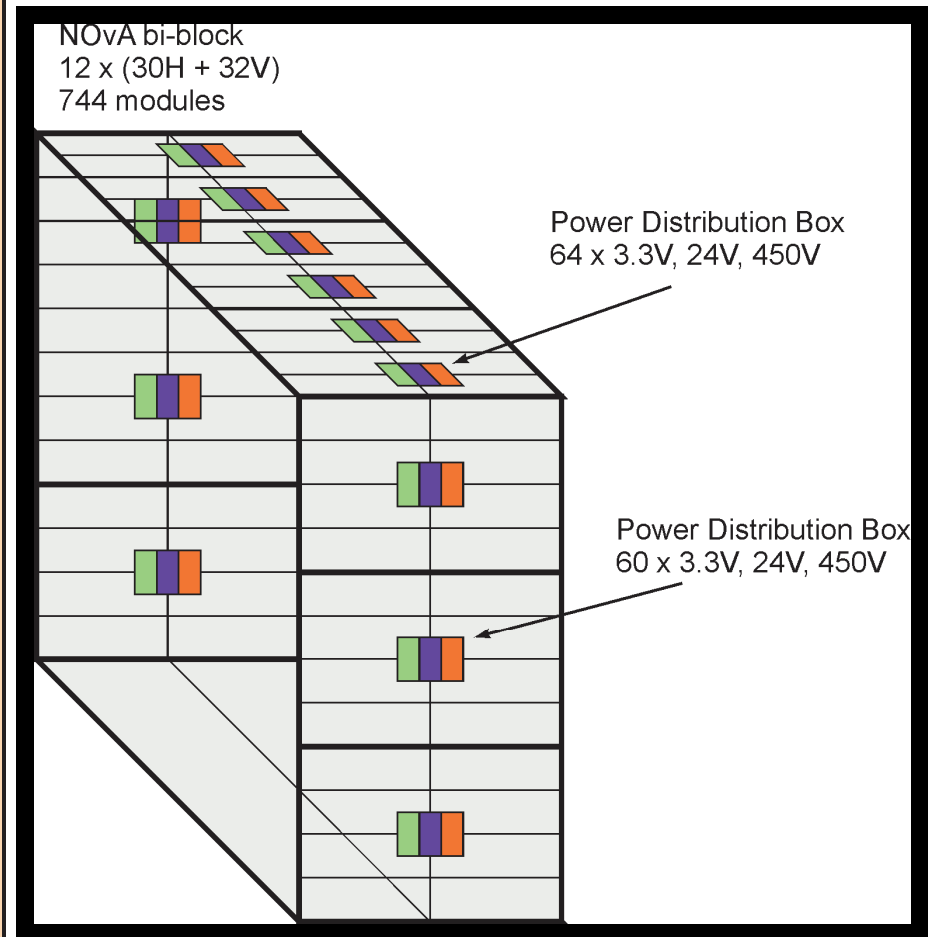
GPS Based Timing System

- The GPS based Timing System consist of:
 - One GPS synchronized master distribution box
 - 32.768Mhz GPS synchronous clock generator
 - Interfaced to the run control host
 - Distributes timing to 24 DCMs
 - 10 Slave distribution boxes
 - Evenly spaced along the backbone of the detector
 - Distributes timing to 24 DCMs
- Timing distribution system implementations being considered
 - Unidirectional timing distribution
 - Bidirectional timing distribution

Number of Power Distribution Boxes

NOvA Electronics Power Supply Requirements

Detector Size (kt)	20	25	30
Blocks	44	54	66
Modules/plane	12	12	12
Horizonatal planes/block	15	15	15
Vertical planes/block	16	16	16
Planes/block	31	31	31
Modules (FEBs)/block	372	372	372
PDBs (DCMs)/block	6	6	6
Total fibers	523,776	642,816	785,664
Total modules (FEBs)	16,368	20,088	24,552
Total PDBs (DCMs)	264	324	396
PDBs/HV channel	2	2	2
HV channels (CAEN)	132	162	198
HV cards (CAEN)	11	14	17
HV cards/mainfraime	8	8	8
HV mainframes (CAEN)	1	2	2
PDBs/3.3V channel	1	1	1
3.3V channels (Weiner)	264	324	396
3.3V channels/mainframe	3	3	3
3.3V mainframes	88	108	132
PDBs/24V channel	1	1	1
24V channels (Weiner)	264	324	396
24V channels/mainframe	3	3	3
24V mainframes	88	108	132



Detector Control Systems

- Lots of investigations
 - UVa, Andrew Norman, looked at many different systems
 - Found some compelling features in EPICS
 - Seriously investigating this
 - Bologna, Niccolo Moggi, also investigating, evaluating solutions, will report soon.

Future

- Designs maturing
 - specification of components allows us to move on to mechanical design, installation, infrastructure requirements.
- Still need work on Open Plan cost and schedule, revisit costs, TDR,